

chip; and

a plurality of second connecting terminals arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive members;

wherein, at least either the first connecting terminals or the second connecting terminals is coupled to a assembly board.

4. A semiconductor device according to claim 3, wherein, one of the first connecting terminals and the second connecting terminals are arranged to be facing to the assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals are made lower than that of another of the first connecting terminals and the second connecting terminals.

5. A semiconductor device according to claim 4, wherein, a portion of either the first connecting terminals or the second connecting terminals are distributed and arranged on the central area of the semiconductor chip, and power source supply potential or ground potential are to be applied thereto.

6. A semiconductor device according to claim 1, further comprising a bonding wire configured to connect at least portion of the connecting terminal that is not used for flip-chip connection with the wiring substrate

of the first connecting terminal and the second connecting terminal in the first semiconductor chip with the third connecting terminal formed on the wiring substrate.

5 7. A semiconductor device according to claim 2,
further comprising a bonding wire configured to connect
at least portion of the connecting terminal that is not
used for flip-chip connection with the lead frame of
10 the first connecting terminal and the second connecting
terminal in the first semiconductor chip with an inner
lead portion of the lead frame.

8. A semiconductor device according to claim 1,
further comprising a second semiconductor chip stacked
on the first semiconductor chip, wherein at least
15 portion of the connecting terminal that is not used for
flip-chip connection with the wiring substrate of the
first connecting terminal and the second connecting
terminal in the first semiconductor chip is coupled to
the second semiconductor chip.

20 9. A semiconductor device according to claim 1,
further comprising a second to an n-th (wherein n is a
positive integer of three or more) semiconductor chips
stacked above the first semiconductor chip, wherein at
least portion of the connecting terminal that is not
25 used for flip-chip connection with the wiring substrate
of the first connecting terminal and the second
connecting terminal in the first semiconductor chip is

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coupled to the second to n-th semiconductor chips.

10. A semiconductor device according to claim 2,
further comprising a second semiconductor chip stacked
on the first semiconductor chip, wherein at least
5 portion of the connecting terminal that is not used for
flip-chip connection with the lead frame of the first
connecting terminal and the second connecting terminal
in the first semiconductor chip is coupled to the
second semiconductor chip.

10 11. A semiconductor device according to claim 2,
further comprising a second to an n-th (wherein n is a
positive integer of three or more) semiconductor chips
stacked above the first semiconductor chip, wherein at
least portion of the connecting terminal that is not
15 used for flip-chip connection with the lead frame of
the first connecting terminal and the second connecting
terminal in the first semiconductor chip is coupled to
the second to n-th semiconductor chips.

12. A semiconductor device according to claim 3,
20 further comprising a second semiconductor chip stacked
on the first semiconductor chip, wherein at least
portion of the connecting terminals arranged on a
stacked surface between the first semiconductor chip
and the second semiconductor chip of the first
25 connecting terminals and the second connecting
terminals in the first semiconductor chip is coupled to
the second semiconductor chip.

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13. A semiconductor device according to claim 3,
further comprising a second to an n-th (wherein n is
a positive integer of three or more) semiconductor
chips stacked above first semiconductor chip, wherein
5 at least portion of the connecting terminals arranged
on a stacked surface between the first semiconductor
chip and the second semiconductor chip of the first
connecting terminals and the second connecting
terminals in the first semiconductor chip is coupled to
10 the second to n-th semiconductor chips.

14. A semiconductor device according to claim 8,
further comprising a bonding wire configured to connect
at least portion of the plurality of connecting
terminals of the semiconductor chips to be stacked with
15 each other.

15. A semiconductor device according to claim 10,
further comprising a bonding wire configured to connect
at least portion of the plurality of connecting
terminals of the semiconductor chips to be stacked with
20 each other.

16. A semiconductor device according to claim 12,
further comprising a bonding wire configured to connect
at least portion of the plurality of connecting
terminals of the semiconductor chips to be stacked with
25 each other.

17. A semiconductor device according to claim 8,
further comprising a conductive bump configured to

18. A semiconductor device according to claim 10,
5 further comprising a conductive bump configured to
connect at least portion of the plurality of connecting
terminals of the semiconductor chips to be stacked with
each other.

20. A semiconductor device comprising:

15 a first semiconductor chip where a semiconductor element is formed;

a conductive member buried in a through hole that goes through the first semiconductor chip;

a second connecting terminal arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive member;

a second semiconductor chip stacked on the first semiconductor chip;

5 a third connecting terminal arranged on a semiconductor element formation surface side in the second semiconductor chip;

10 wherein, one of the first connecting terminal and the second connecting terminal of the first semiconductor chip is arranged at a position facing to the third connecting terminal of the second semiconductor chip, the first semiconductor chip and the second semiconductor chip are electrically connected with each other through the facing connecting terminals, and

15 the second semiconductor chip is thicker or larger than the first semiconductor chip.